4th IEEE Workshop on Signal Propagation on Interconnects
Magdeburg, Germany, May 17-19, 2000

Efficient Time Domain Simulation and Parameter Extraction Team Up to Describe High Speed IC Packages

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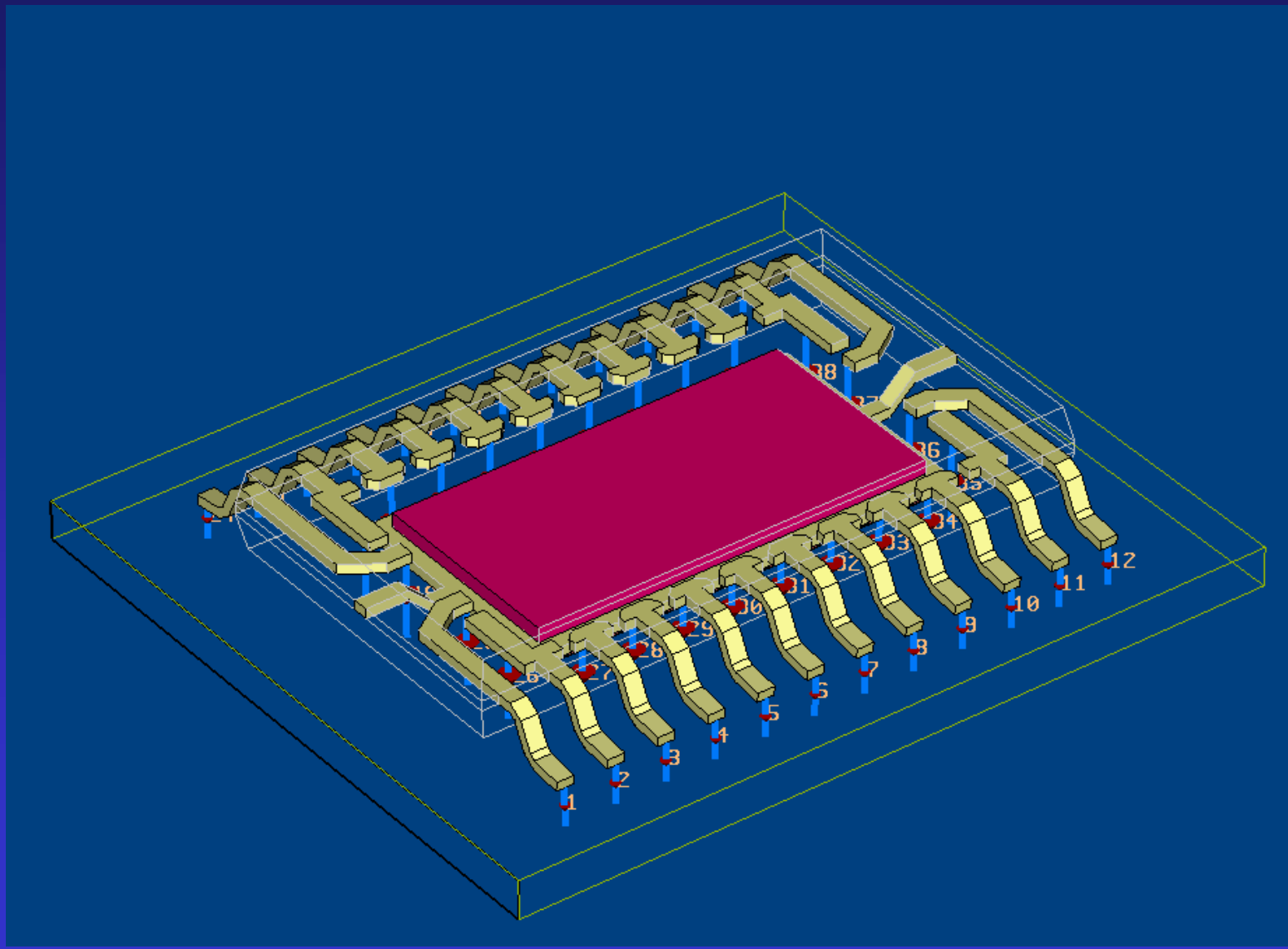
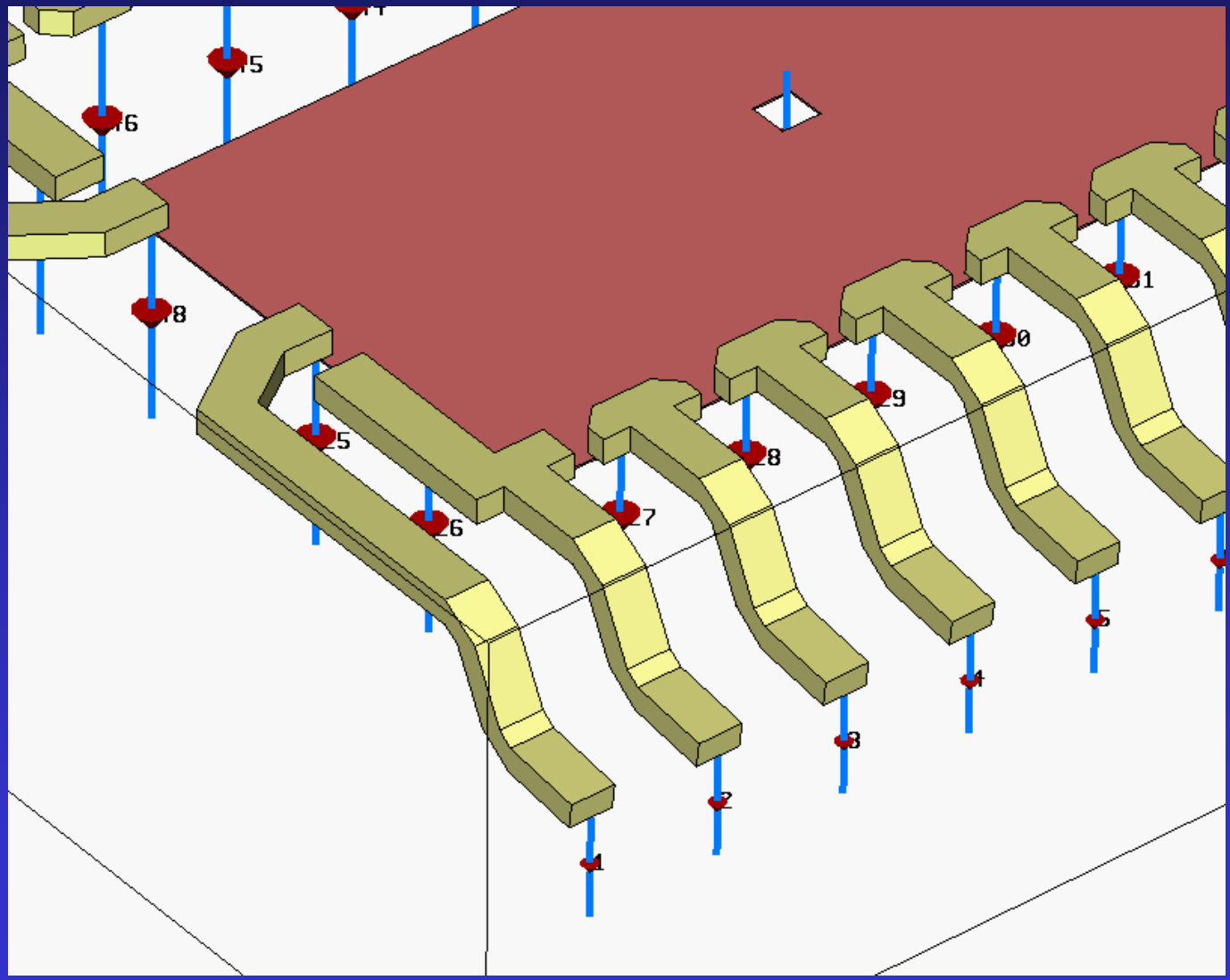
Abstract:

At high frequencies the parasitic effects of packages on the performance of integrated circuits cannot be ignored, since e.g. the serial inductance, mutual capacitances and inductances between lead frame, bond wires and pins have serious influence. It is best, when these effects are taken into account as early as possible in the design phase. Accurate equivalent circuit models are vital to describe these effects. The method presented here is based on S-parameters computed by a 3D finite integration technique to extract the parameters of the equivalent circuits for the whole package. SPICE equivalent circuit and their corresponding S- parameters are compared to the broadband S- parameters derived from the time domain simulation for a P-TSSOP24 IC - Package from Infineon Technologies AG.

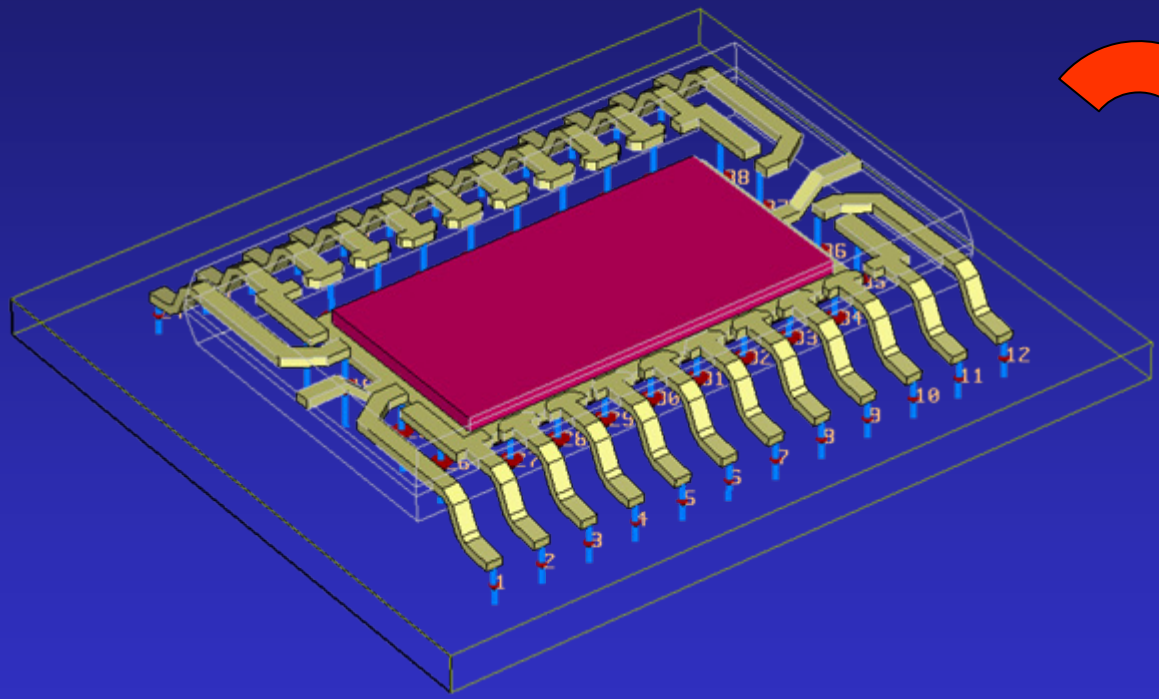
The Model: P-TSSOP24

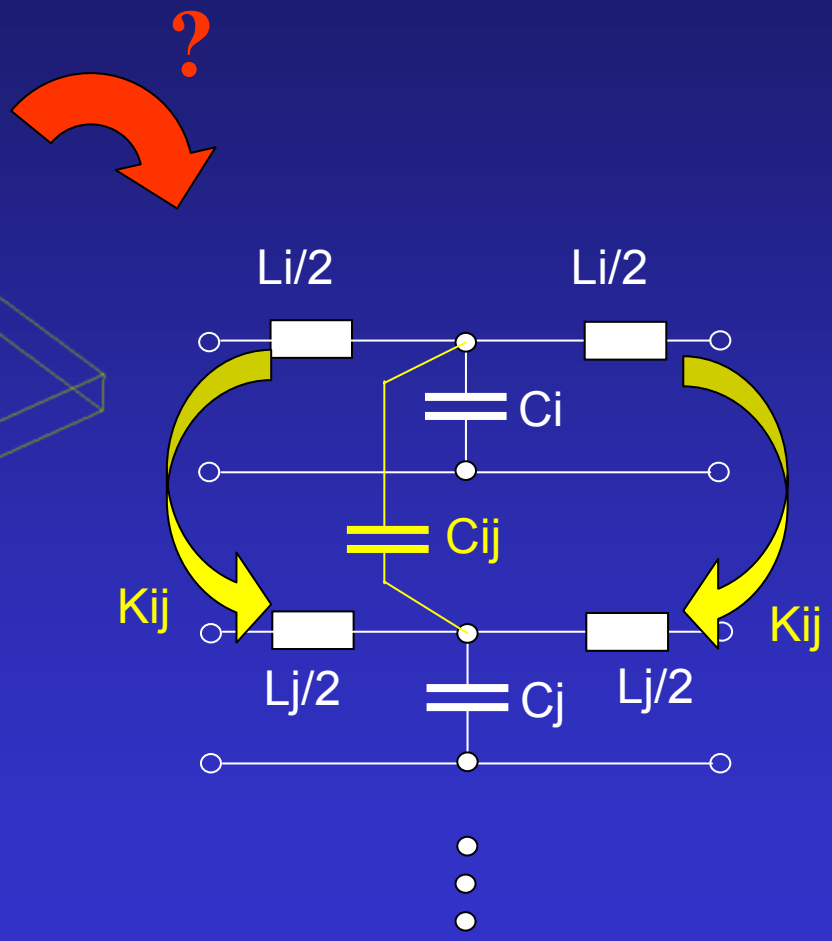


The Model: P-TSSOP24, Close-Up Look at the Leadframe and Ports



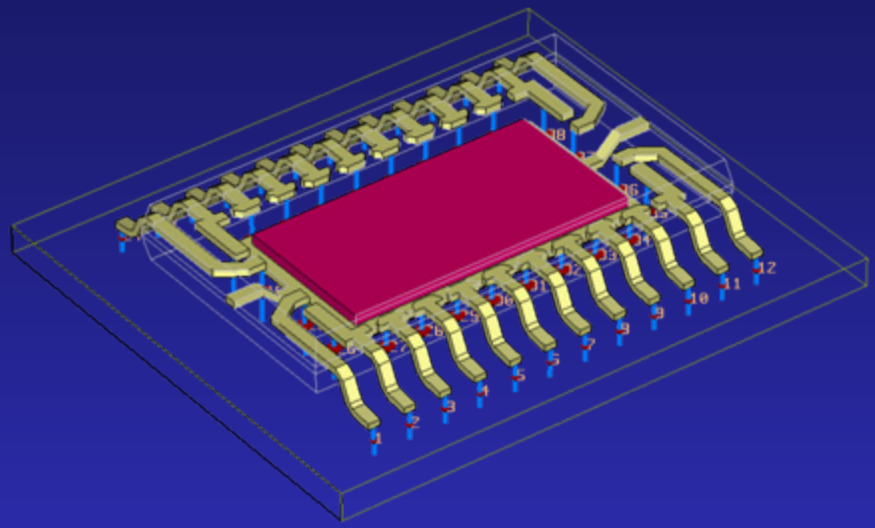
SPICE Model Extraction using an Equivalent Circuit





Describe the 3D structure by an equivalent discrete network.

SPICE Model Extraction



Extraction principles:

- Static extraction
- Dynamic extraction

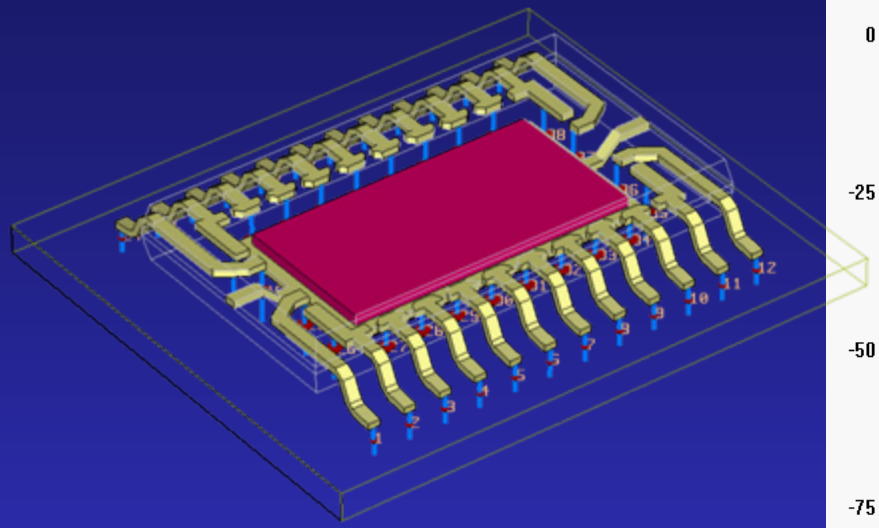
Static extraction

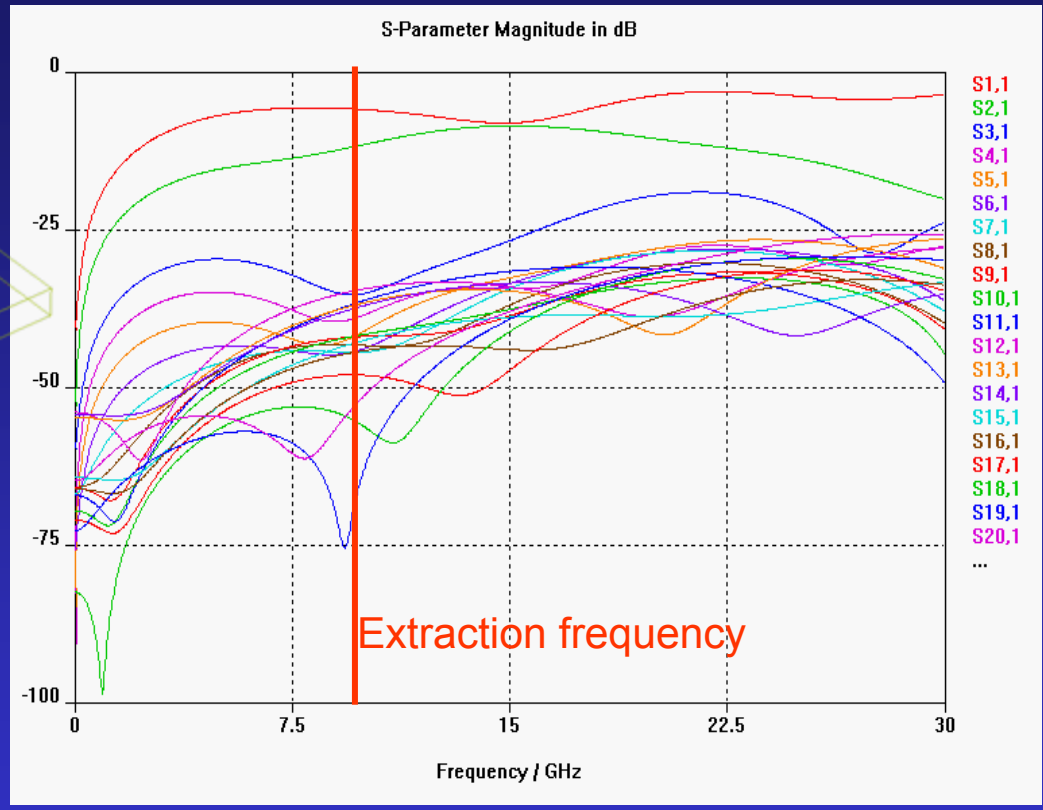
- Requires static E and B calculations.
- Computes SPICE network from L, C matrices.
- Contains no dynamic effects

Dynamic extraction

- Requires dynamic EM calculations
- Computes SPICE network from S-Parameters
- Allows cascaded networks

SPICE Model Extraction





24 “wires”,
total simulation time 35 min.

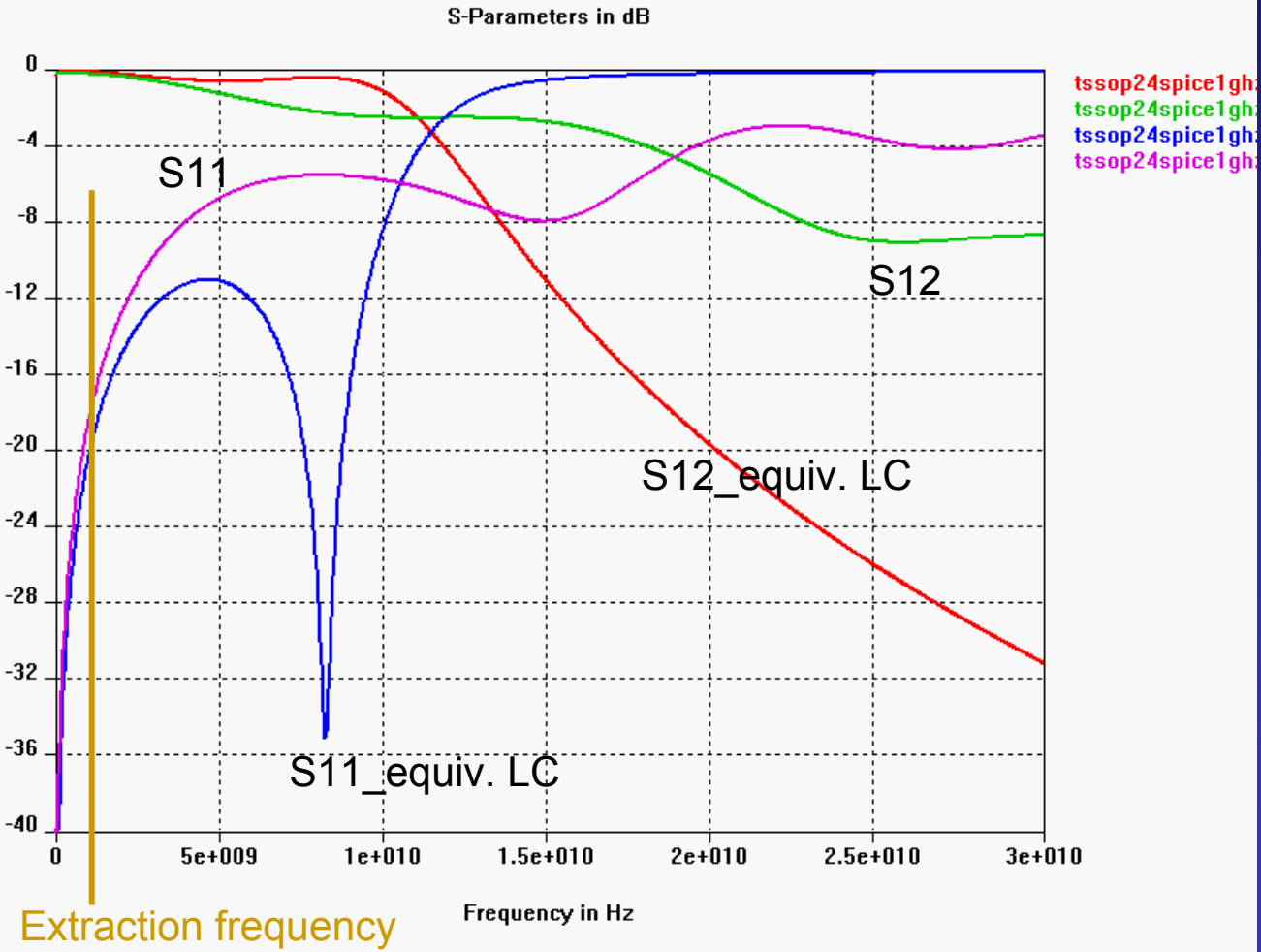
The SPICE model is extracted from the complex S-parameters at the extraction frequency

SPICE Model: Circuit-Description

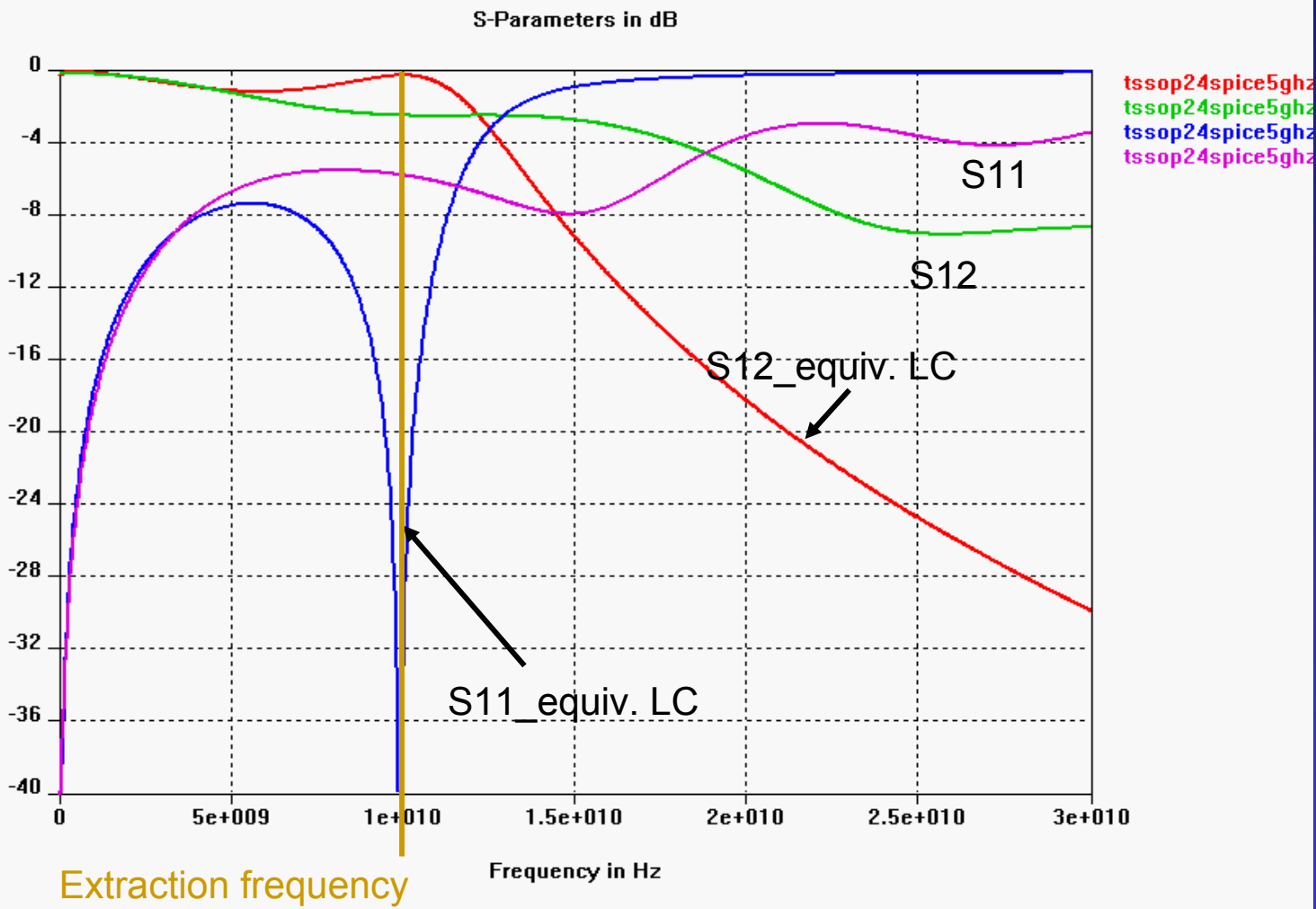
SPICE Circuit description generated by
CST MicroWaveStudio

```
.ac LIN 999 15000000 15000000000

L11     11 10 1.27112e-009
L12     10 12 1.27112e-009
C1      10 0 2.38794e-013
L21     21 20 9.47191e-010
L22     20 22 9.47191e-010
C2      20 0 2.3486e-013
. . .

C24     240 0 2.4791e-013
C1_2    10 20 1.05825e-013
K11_2   L11 L21 0.221087
K21_2   L12 L22 0.221087
C1_3    10 30 9.09917e-015
K11_3   L11 L31 0.0647162
K21_3   L12 L32 0.0647162
. . .

R11     11 0 50
R12     12 0 50
R21     21 0 50
R22     22 0 50
R31     31 33 50
. . .
VV      33 0 DC 0V AC 1
R32     32 0 50

.width out=132
.print ac vr(11) vi(11) vr(12) vi(12)
.print ac vr(21) vi(21) vr(22) vi(22)
.print ac vr(31) vi(31) vr(32) vi(32)
. . .
.print ac ir(vv) ii(vv)

.end
```

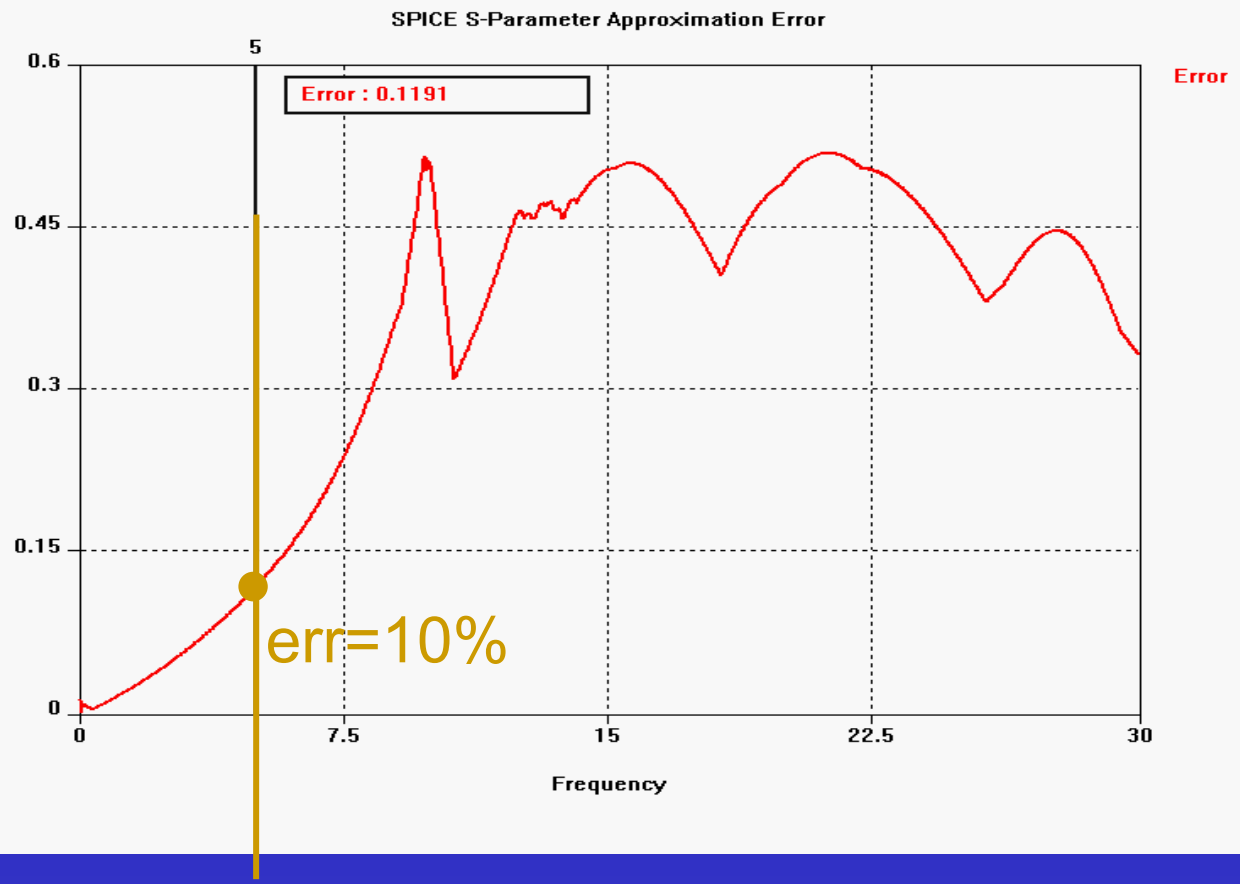

Comparison between S-Parameters of 3D EM and Spice at 1 GHz



Comparison between S-Parameters of 3D EM and Spice at 10 GHz



Error of SPICE Model Approximation

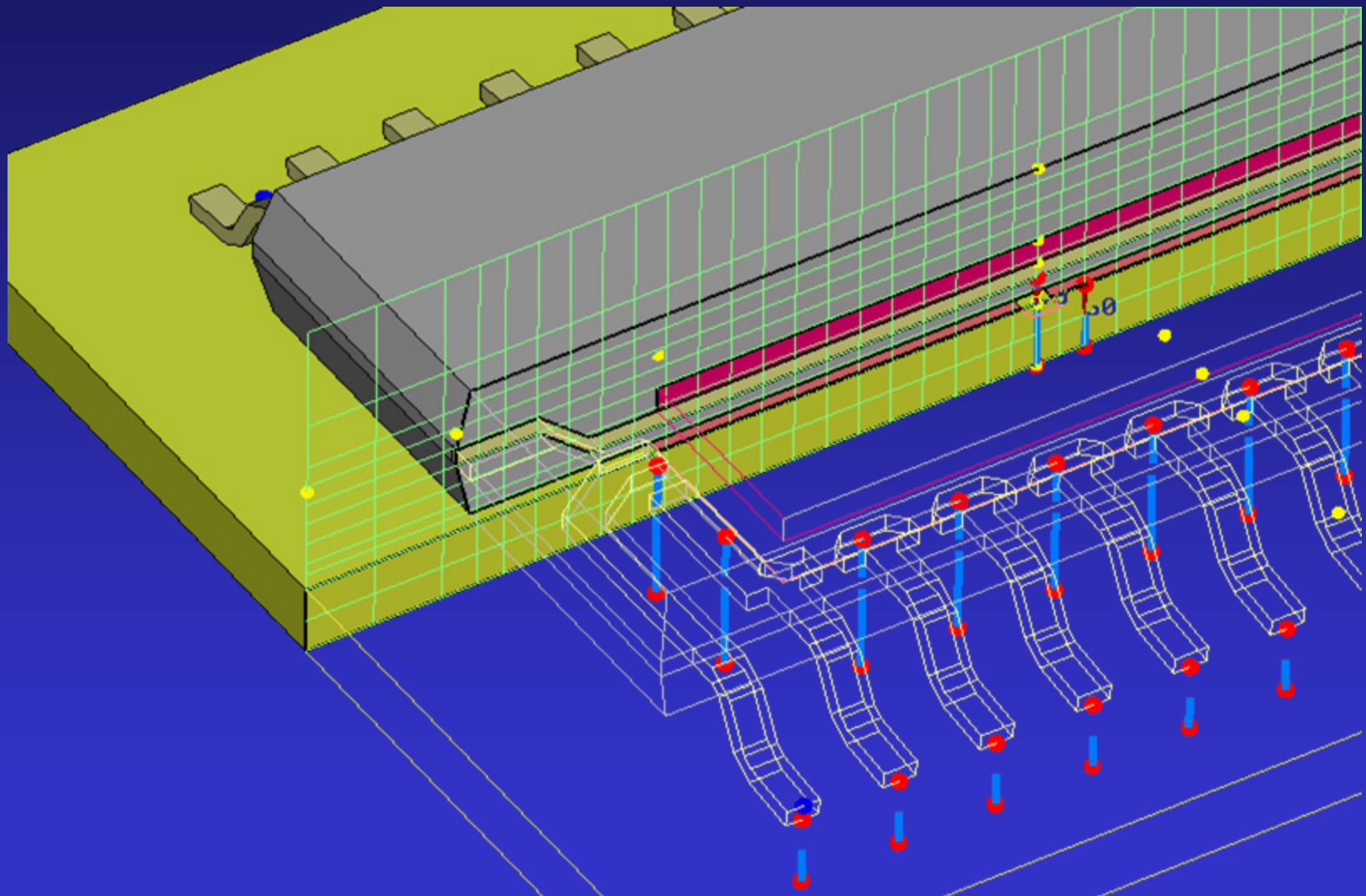


Error increases with frequency

Conductor length = λ/10

$$\text{error (frequencies)} = \max_{\text{wires ij}} \{ |V_{s\_parameter} - V_{Spice}| \}$$

Meshdetails shown at a Vertical Cutplane



S-Parameter Extraction: Runtime Statistics for the P-TSSOP24

Solver Statistics:

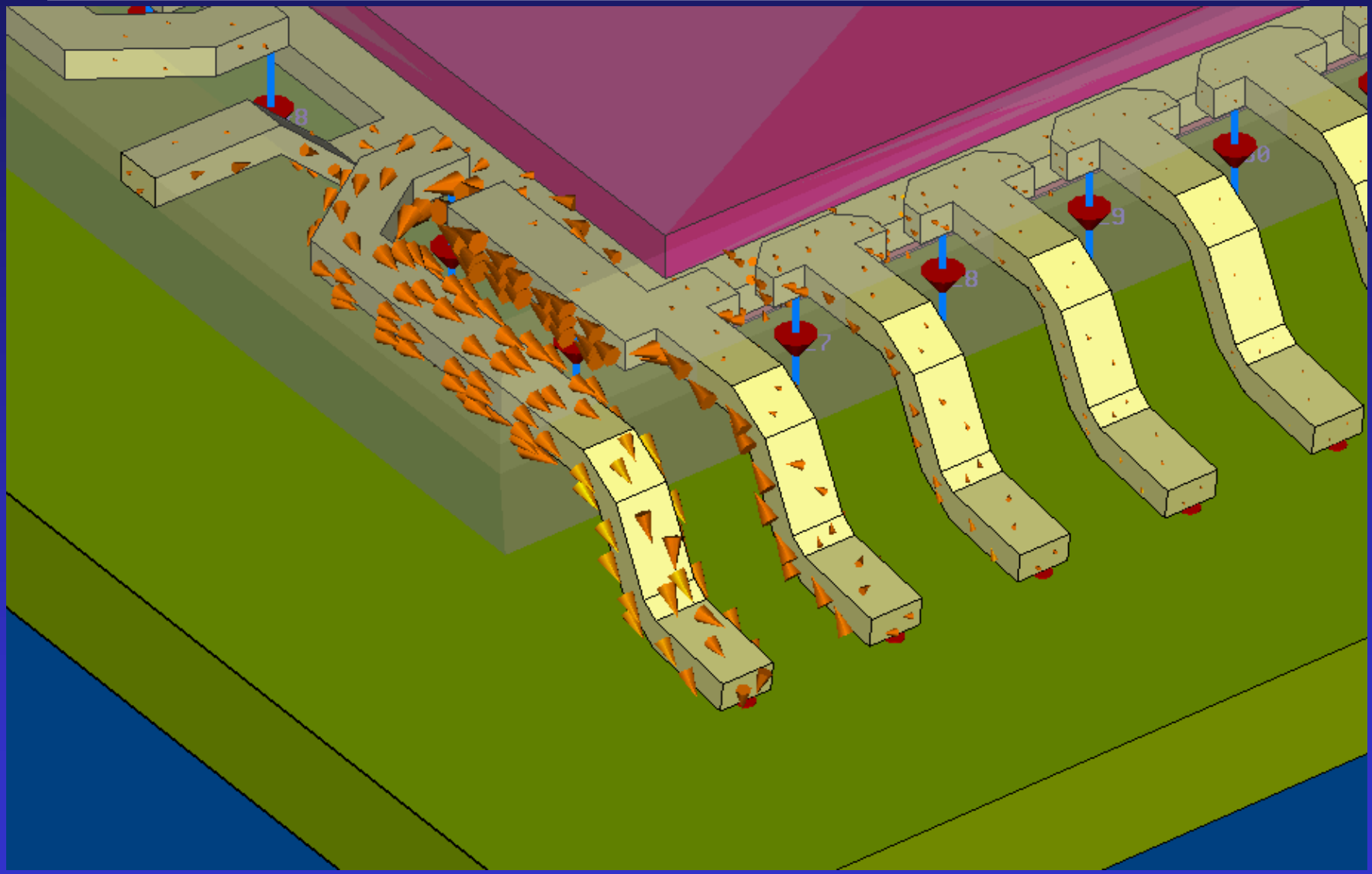
Number of nodes:	23736	
Number of time steps:	781	
Time step width:	2.510138e-004 ns	
Time step factor:	1.1264	
Mesh generation time:	120	s
Solver time:	82	s / Port

Time for all Ports: 82 s * 24 ports = 33 min

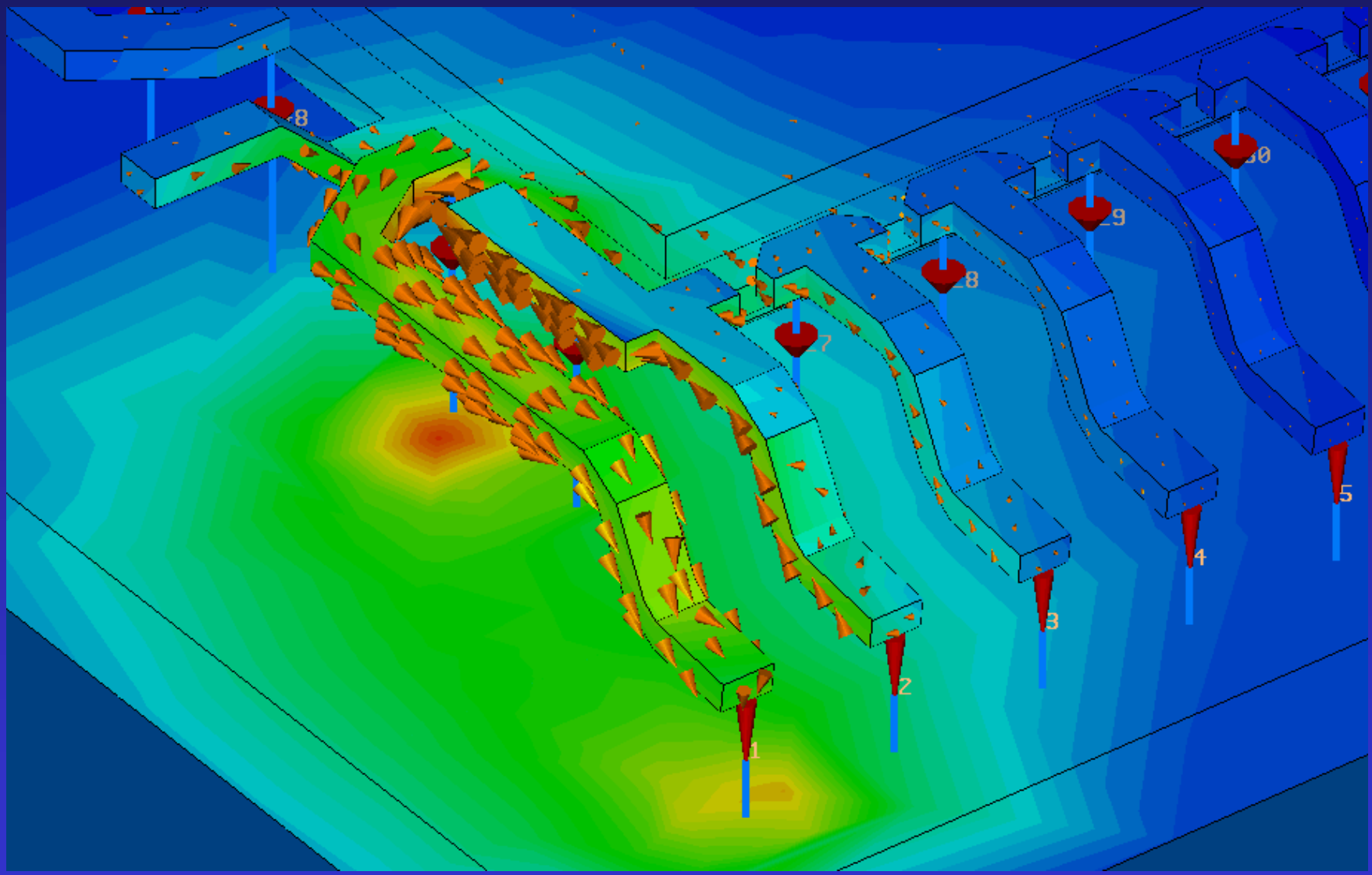
Total Time: **35 min !**

Averaged performance: 7.7 MFLOP/s

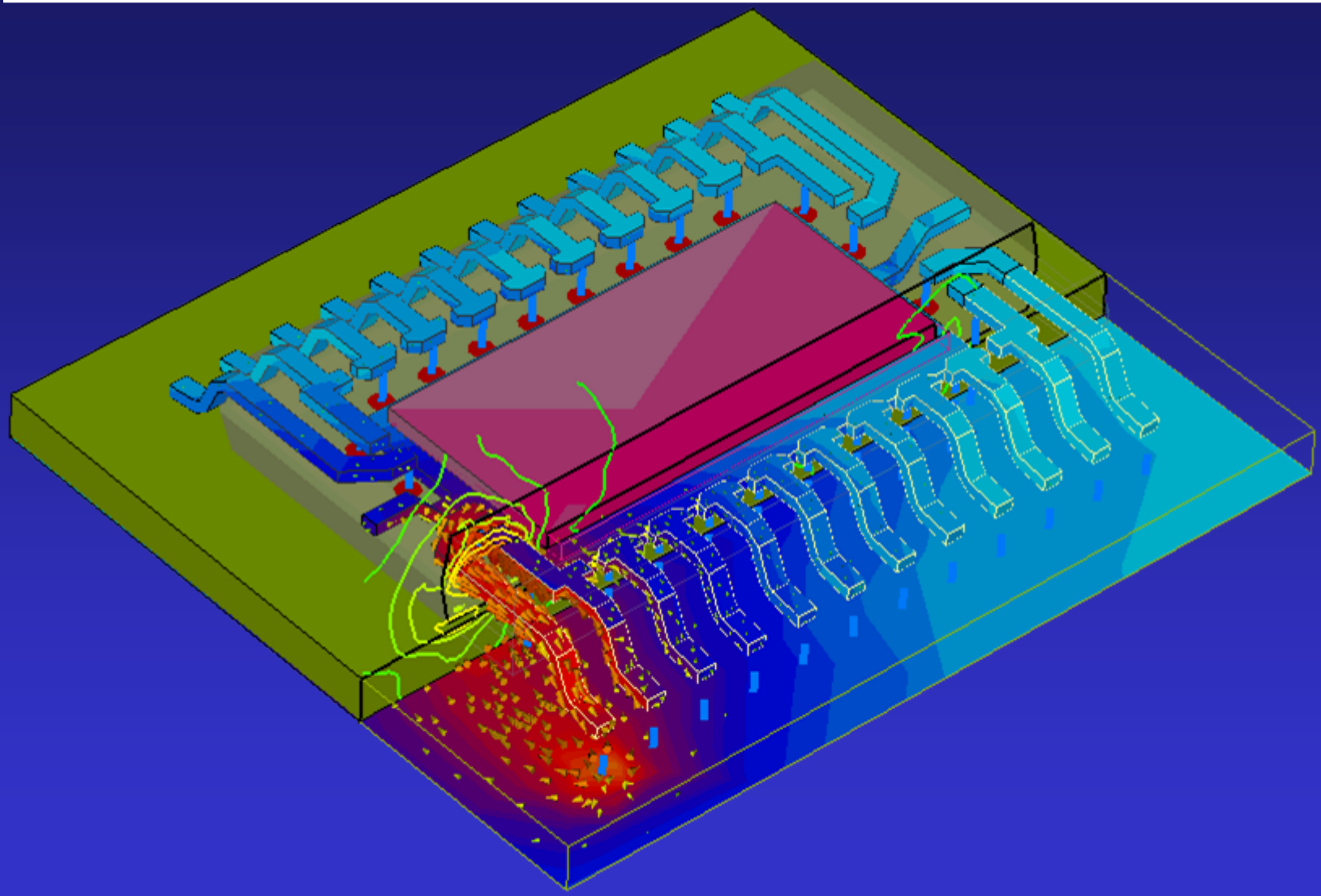
Arrowplot of the Surface-Current-Density at 5 GHz



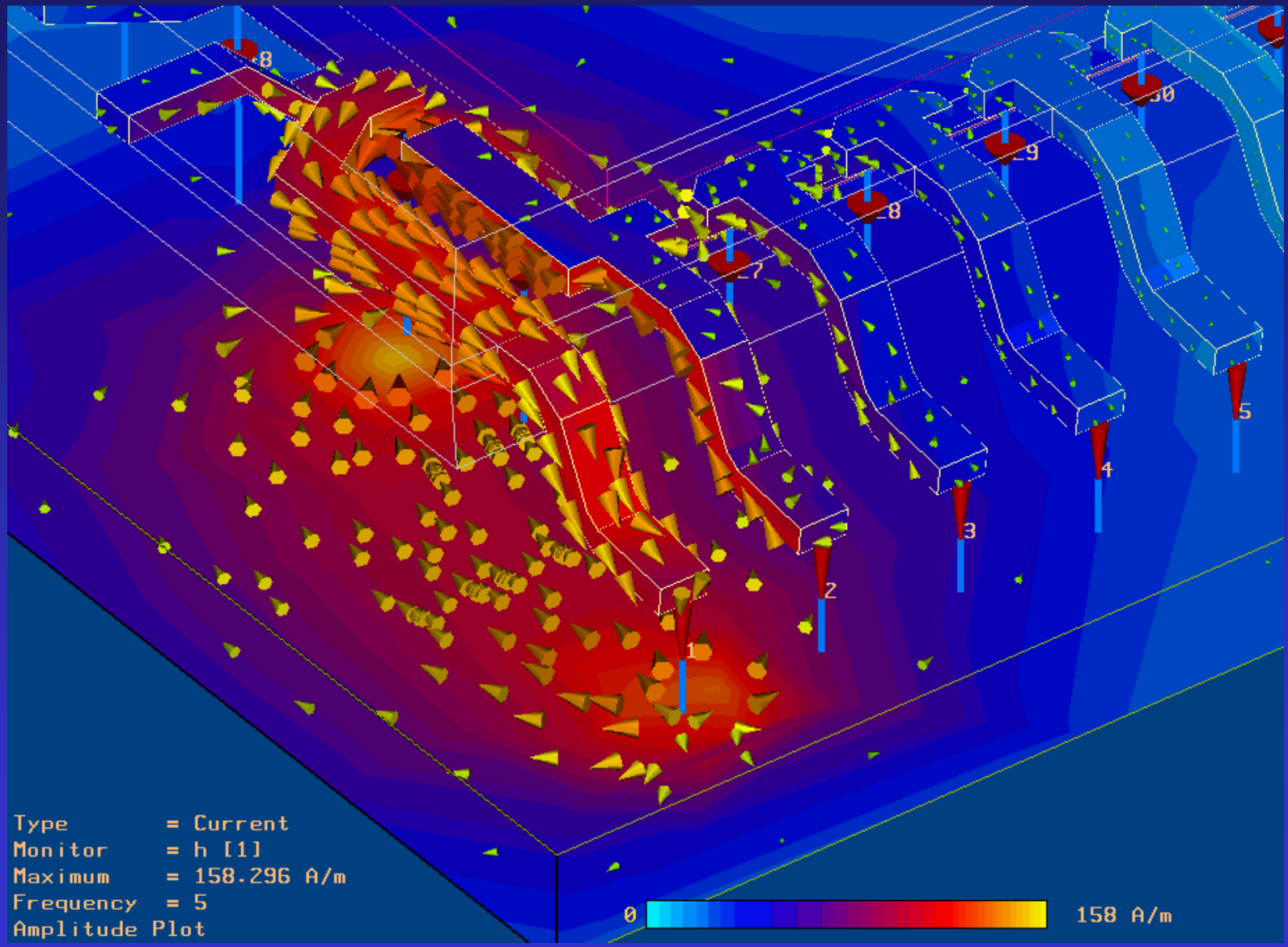
Combined Arrow- / Contourplot of the Surface-Current-Density at 5 GHz



Surface-Current-Density and E-Contourlines at 5 GHz



Contour/Arrowplot of the Surface-Current-Density at 5 GHz



SPICE Model Extraction vs. Digital EM-Simulation

The error increases with frequency

→ Cascading the equivalent network improves approximation of higher frequencies

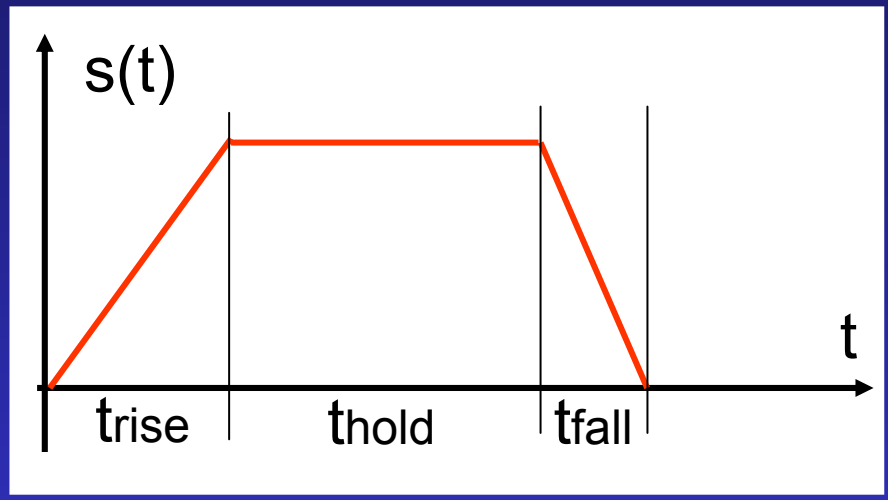
Equivalent networks become increasingly complex with frequency

→ Practical limitation of this method for higher frequencies (high speed digital circuits)

→ True “digital” EM simulation becomes necessary

Digital Signal Simulation

"Digital" Excitation Signal (simple)



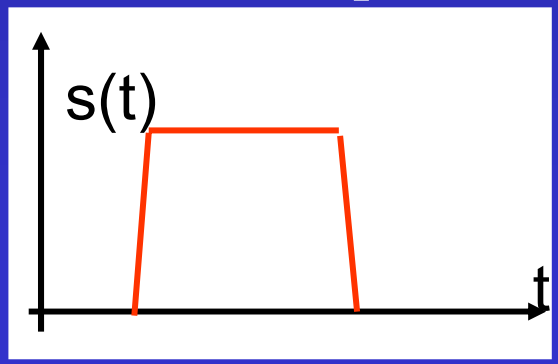
"Low clock speed":

$t_{rise}, t_{fall} \ll t_{hold}$

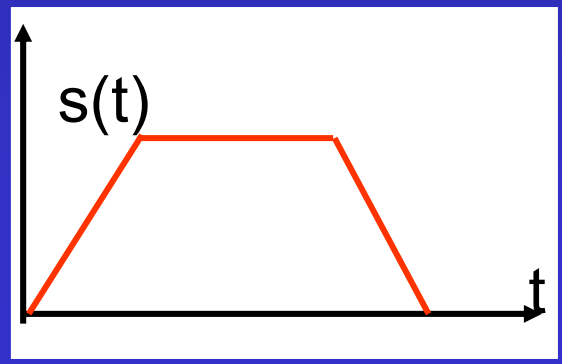
"High clock speed":

otherwise

"Low clock speed"



"High clock speed"



Digital Signal Simulation

Simulation of digital systems

1. True “digital” EM simulation

+ Most flexible approach, accurate high frequency results
+ Can handle non linearity's
- Slow for low clock speed systems (time step is fixed)

2. Calculation of “digital” response from S-parameters

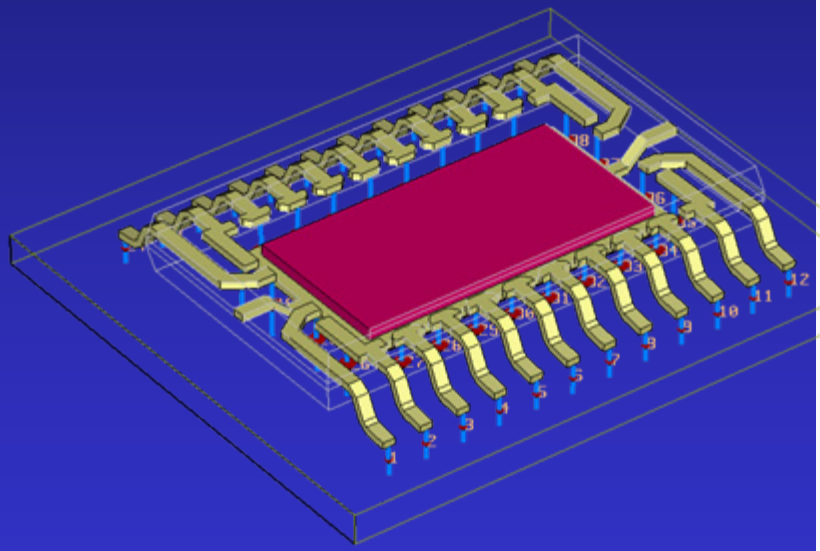
+ Accurate high frequency results
+ Fast even for low clock speed systems
- Can not handle non linearity's

3. Calculation of “digital” response from SPICE model

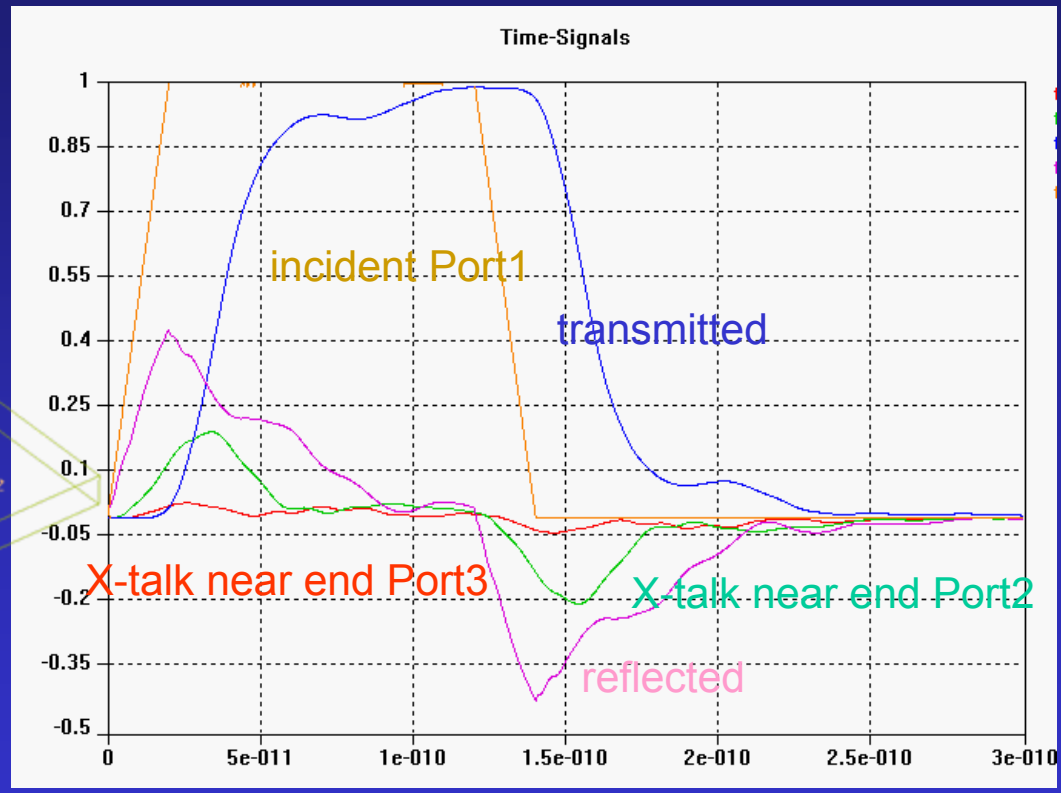
+ Can handle non linearity's
+ Fast even for low clock speed systems
- Inaccurate high frequency results

Digital Signal Simulation

True “Digital” simulation



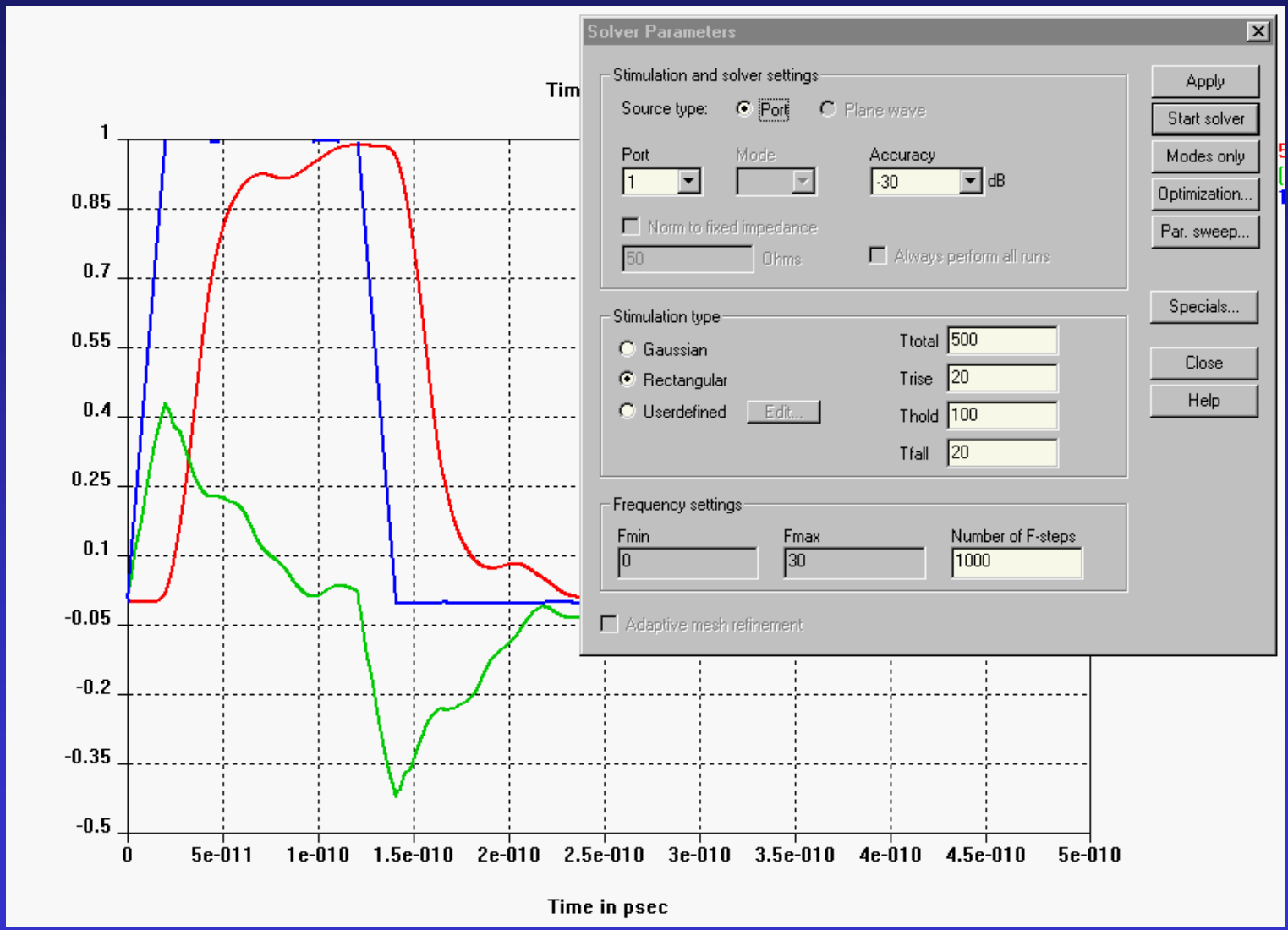
Transmission, Reflection and Cross talk



24 “wires”,
total simulation time = 6 min / excitation

Small cross talk because of grounded layer.

Digital Signal Simulation: Easy Setup of Excitation Shapes



Transient Runtime Statistics for the P-TSSOP24

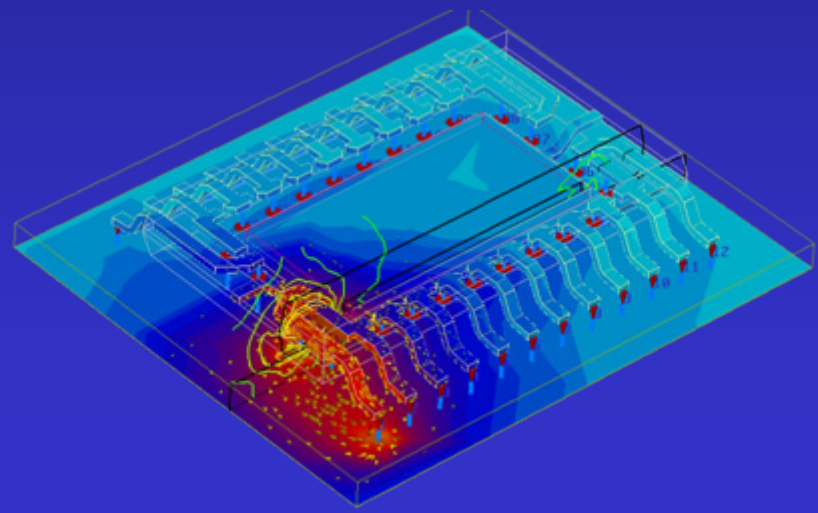
Solver Statistics:

Number of nodes:	23736	
Number of time steps:	1991	
Time step width:	2.510138e-001 ps	
Time step factor:	1.1264	
Mesh generation time:	1	s
Solver time:	350	s

Total time:	351	s / Port
Averaged performance:	4.6	MFLOP/s

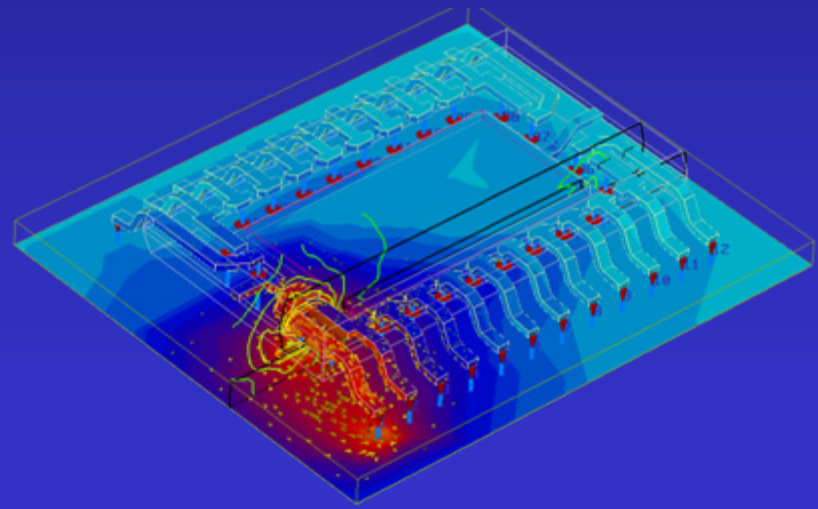
Conclusions

* Fast and accurate dynamic S-Parameter computation
* Spice Parameter extraction
* Built-in Comparison between EM/Spice S-Parameters
* True EM-Digital Simulation possible
*
*
*

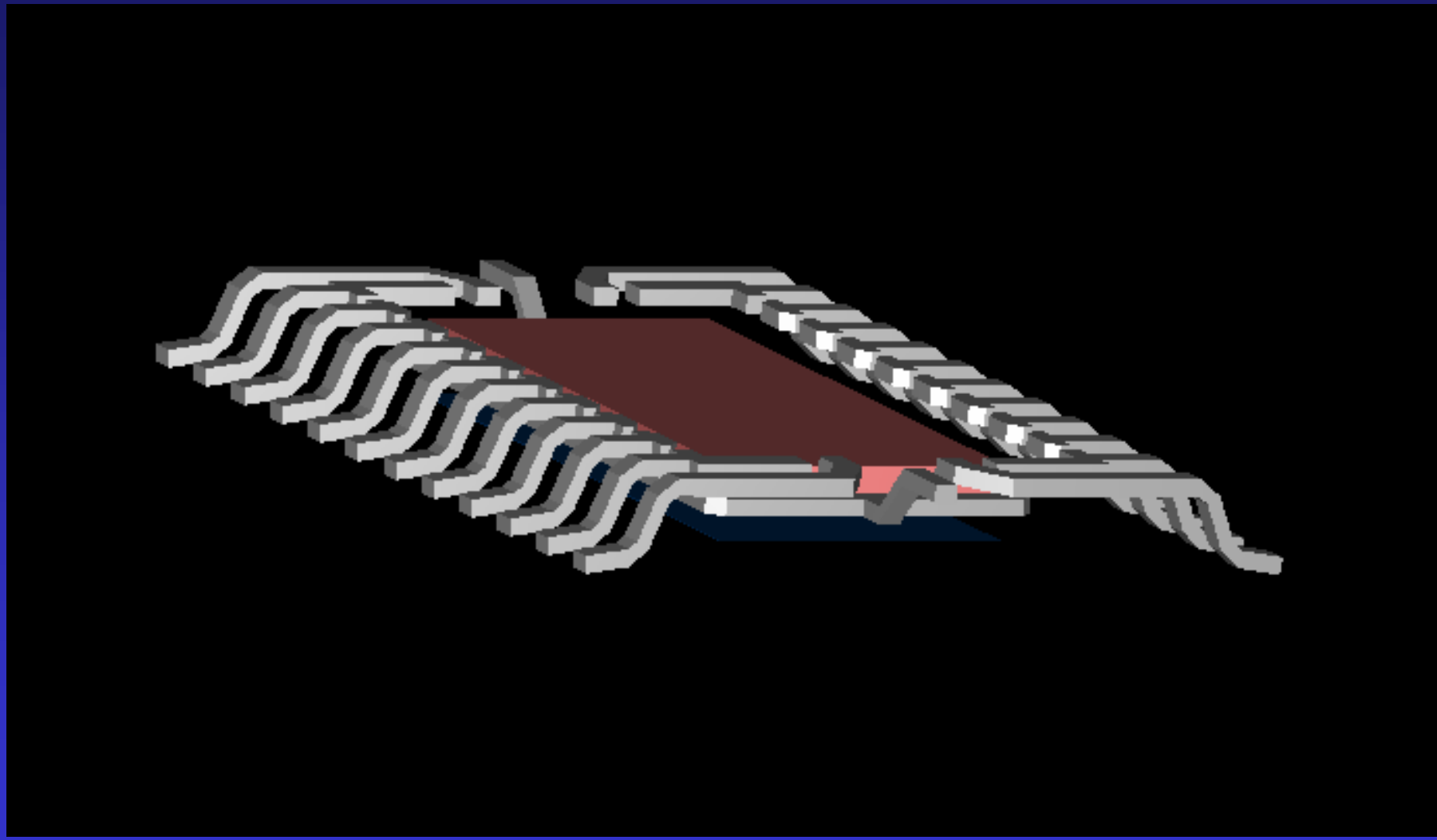


Future Enhancements

* Extension of the Equivalent Circuit Model to take dielectric losses and ohmic losses into account
* More complex built-in Circuit Models
* TDR ...
*
*



ACIS - Previewer allows dynamic operations



If Previewer is installed double-click on the image